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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/606,715

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Benjamin Thomas Percer

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11/16/2007

HEWLETT PACKARD COMPANY

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INTELLECTUAL PROPERTY ADMINISTRATION

FORT COLLINS, CO 80527-2400

EXAMINER

LE, JOHN H

ART UNIT

PAPER NUMBER

2863

MAIL DATE

DELIVERY MODE

11/16/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/606,715	Applicant(s) PERCER ET AL.	
	Examiner John H. Le	Art Unit 2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5, 6, 8-10, 12-21 and 24-30 is/are pending in the application.
 4a) Of the above claim(s) 4, 7, 11, 22, 23, 31 and 32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 6, 8-10, 12-21 and 24-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

1. Applicant's amendment filed 10/16/2007 has been entered and carefully considered.

Claims 1, 8, 12, 14-15, 18, 24, and 28 have been amended.

Claims 4, 7, 11, 22-23, 27, and 31-32 have been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-6, 8-9, 13, 15-17, 24-26, and 29- 30 are rejected in the alternative, under 35 U.S.C. 103(a) as obvious over Coyle et al. (USP 6,546,507).

Regarding claims 1 and 24, Coyle et al. disclose a system for margin testing one or more components of an electronic system (computer's bus system)(Fig.25, Col.33, lines 8-13, Col.34, lines 7-20), comprising a fault bypass module (a failure capture module 2506) incorporated in said electronic system (bus 2502), said fault bypass module (failure capture module 2506) configured to intercept at least one signal (e.g. Fig.25, Col.34, lines 56-65, Col.39, line 42-Col.40, line 12) to indicate of one or more faults associated with one or more of said components (bus 2502) during margin testing of said electronic system (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34) and mask the at least one signal indicative of one or more faults (the

system does not pass the value) by generating at least one signal indicative of absence of the one or more faults (the system passes the value, it is inherently teach the system bus does not have any faults or generating at least one signal indicative of absence of the one or more faults (signal indicate the system pass the value) in the system bus, it is inherently teach hiding or masking the signal indicate of one or more faults) (e.g. Figs.28C, 28D, Col.39, line 42-Col.40, line 12); an internal controller (a program control module 2512) in said electronic system and in communication with said fault bypass module (failure capture module 2506), said internal controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module (e.g. Fig.25, Col.34, lines 62-65, Col.39, line 42-Col.40, line 12); and a hardware monitor (stress injection module 2504) configured to communication with said controller (program control module 2512) and with at least one of said one or more components (failure capture module 2506), and to generate a fault signal in response to an occurrence of a fault associated with said at least one component (failure capture module 2506) (e.g. Fig.25, Col.35, lines 5-30).

Although Coyle et al. is silent on the teaching wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold, however it would have been obvious to one of ordinary skill at the time the invention was made to teach the hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold since Coyle et al. disclose hardware

monitor (stress injection module 2504) configured to communication with said controller (program control module 2512) and with at least one of said one or more components (failure capture module 2506), and to generate a fault signal in response to an occurrence of a fault associated with said at least one component (failure capture module 2506) (e.g. Fig.25, Col.35, lines 5-30); said fault bypass module (failure capture module 2506) configured to intercept at least one signal (e.g. Fig.25, Col.34, lines 56-65, Col.39, line 42-Col.40, line 12) to indicate of one or more faults associated with one or more of said components (bus 2502) during margin testing of said electronic system (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34); at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold (e.g. Col.35, lines 50-65); and a voltage associated with a power rail (e.g. Col.17, lines 49-63) for purpose of providing a system for margin testing one or more components of an electronic system (computer's bus system)(Fig.25, Col.33, lines 8-13, Col.34, lines 7-20) as intended.

Regarding claim 2, Coyle et al. disclose at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold (e.g. Col.35, lines 50-65).

Regarding claim 3, Coyle et al. disclose said operating parameter is any of voltage (e.g. Col.35, lines 50-65).

Regarding claim 5, Coyle et al. disclose said fault signals comprise one or more interrupt signals (e.g. Col.14, lines 36-48, Col.30 lines 60-63, Col.44, lines 28-32).

Regarding claim 6, Coyle et al. disclose said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system (e.g. Col.9, lines 35-39, Col.37, lines 28-32).

Regarding claim 8, Coyle et al. disclose said hardware monitor (stress injection module 2504) is further configured to transmit said fault signal to said fault bypass module (failure capture module 2506), and wherein said fault bypass module (failure capture module 2506) is further configured to mask said received fault signal during margin testing of said electronic device (e.g. Fig.25, Col.35, lines 5-30, Col.36, lines 23-29).

Regarding claims 9 and 25, Coyle et al. disclose a power control element (program control module 2512 (JTAG controller), Fig.16, Col.22, line 51-Col.23, lines36) in communication with said fault bypass module (2506), said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system (the system pass the value, it is inherently teach the system bus is not fault or generating at least one signal indicative of absence of the one or more faults (pass the value) in the system bus, it is inherently teach hiding or masking the signal indicate of one or more faults) (e.g. Fig.25, Col.34, lines 50-65, Col.39, line 42-Col.40, line 12).

Regarding claim 10, Coyle et al. disclose said fault bypass module (failure capture module 2506) masks said fault signal by intercepting (capturing) said fault signal (e.g. Fig.25, Col.34, lines 56-65, Col.39, line 42-Col.40, line 12) and supplying to

said power control element (2512) (e.g. Fig.25, Col.34, lines 50-65) a signal indicative of absence of a fault indicated by said fault signal (the system pass the value, it is inherently teach the system bus is not fault or generating at least one signal indicative of absence of the one or more faults (pass the value) in the system bus, it is inherently teach hiding or masking the signal indicate of one or more faults) (e.g. Fig.25, Col.34, lines 50-65, Col.39, line 42-Col.40, line 12).

Regarding claims 12 and 28, although Coyle et al. is silent on the teaching wherein said power control module is further configured to reduce power applied to said power rail in response to said interrupt signal in the absence of margin testing; however it would have been obvious to one of ordinary skill at the time the invention was made to teach said power control module is further configured to reduce power applied to said power rail in response to said interrupt signal in the absence of margin testing since Coyle et al. disclose said fault bypass module (failure capture module 2506) configured to intercept at least one signal (e.g. Fig.25, Col.34, lines 56-65, Col.39, line 42-Col.40, line 12) to indicate of one or more faults associated with one or more of said components (bus 2502) during margin testing of said electronic system (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34) and mask the at least one signal indicative of one or more faults (the system does not pass the value) by generating at least one signal indicative of absence of the one or more faults (the system passes the value, it is inherently teach the system bus does not have any faults or generating at least one signal indicative of absence of the one or more faults (signal indicate the system pass the value) in the system bus, it is inherently teach hiding or

masking the signal indicate of one or more faults) (e.g. Figs.28C, 28D, Col.39, line 42-Col.40, line 12) and reducing power applied to power rail ((e.g. Col.17, lines 49-63) for purpose of providing a system for margin testing one or more components of an electronic system (computer's bus system)(Fig.25, Col.33, lines 8-13, Col.34, lines 7-20) as intended.

Regarding claim 13, Coyle et al. disclose a programmable logic device (FFM logic 120) programmed to provide masking of said fault signals (the system pass the value, it is inherently teach the system bus is not fault or generating at least one signal indicative of absence of the one or more faults (pass the value) in the system bus, it is inherently teach hiding or masking the signal indicate of one or more faults) (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-26), Col.39, line 42-Col.40, line 12).

Regarding claims 15 and 29, Coyle et al. disclose said fault bypass module (failure capture module 2506) is further configured to intercept a selected output signal of said at least one component and to generate a simulated signal corresponding to said intercepted output signal (e.g. Col.14, lines 36-48, Col.30 lines 60-63, Col.44, lines 28-32) for transmittal to said hardware monitor (stress injection module 2504) during margin testing of said component (e.g. Fig.25, Col.35, lines 5-30, Col.36, lines 23-29).

Regarding claim 16, Coyle et al. disclose said electronic system comprises a computer system (e.g. Col.31, lines 31-35, Col.32, lines 59-62).

Regarding claim 17, Coyle et al. disclose computer system is a computer server (e.g. Col.31, lines 21-23).

Regarding claim 30, Coyle et al. disclose said electronic system is a computer server (e.g. Col.31, lines 21-23, 31-35, Col.32, lines 59-62).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al. (USP 6,546,507) in view of Taraci et al. (USP 5,119,021).

Regarding claim 14, Coyle et al. fail to disclose a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor.

Taraci et al. teach a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor (e.g. Col.6, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor as taught by Taraci et al. in a margin test method of Coyle et al. for the purpose of providing a method and apparatus for maintaining a desired case temperature of an electrically operating device undergoing a burn-in test (Taraci et al., Col.3, lines 65-68).

5. Claim 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al. (USP 6,546,507) in view of Hawkins et al. (US 2003/0130969 A1).

Regarding claims 18-21, Coyle et al. fail to disclose a controller comprises a Baseboard Management Controller (BMC), wherein said communication bus is an Inter-

Integrated Circuit bus (I²C bus), wherein said I²C bus is Intelligent Platform Management Bus (IPMB).

Hawkins et al. disclose a controller comprises a Baseboard Management Controller (BMC) ([0015]-[0017]), wherein said communication bus is an Inter-Integrated Circuit bus (I²C bus)([0006]), wherein said I²C bus is IPMB ([0013]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Baseboard Management Controller (BMC), an Inter-Integrated Circuit bus (I²C bus), wherein said I²C bus is Intelligent Platform Management Bus (IPMB) as taught by Hawkins et al. in a margin test method of Coyle et al. for the purpose of providing a star Intelligent Platform Management Bus Topology.

Response to Arguments

6. Applicant's arguments with respect to claims 1-3, 5-6, 8-10, 12-21, and 24-30 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is 571 272 2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571 272 2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "John Le", with a stylized flourish at the end.

John H. Le

Patent Examiner-Group 2863

November 6, 2007